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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/693,928
Filing Date: October 28, 2003
Appellant(s): OKADA ET AL.

Alan J Kasper
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/29/2007 appealing from the Office action mailed 2/5/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is substantially correct.

Claims 2, 6, 7, 9, 10, 13, 14, and 16 are no longer finally rejected and are instead objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. The 35 U.S.C. 103(a) rejections of claims 2, 6, 7, 9, 10, 13, 14, and 16 have been withdrawn.

Claims 2, 6, 7, 9, 10, 13, 14, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2002/0051415 A1		Iijima	5-2002
2004/0090889	A1	Okada et al.	5-2004
(Applicant's Admitted Prior		Applicant's Figure 15 and	

Art, herein AAPA)	corresponding description	
6,493,305 B1	Hayashi et al.	12-2002
5,818,805	Kobayashi et al.	10-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima (US PGPub 2002/0051415 A1) and further in view of Applicants Admitted Prior Art (hereafter AAPA). It is noted that citations to AAPA refer to the Background of the Invention of Applicant's Specification.

Regarding claim 1, Iijima discloses a recording pulse generator comprising: a first delay line having plural circuit elements cascaded in multiple stages, wherein the first delay line outputs plural output clocks each having different phase differences with a clock inputted to the first stage of the first delay line, according to the number of stages of the plural circuit elements thereof (see Figure 1 element 11 and the discussion in paragraph [0033]). Iijima also discloses a selector that is used to select an arbitrary clock from the plural clocks generated (Figure 1 element 12 and further paragraph [0034]) and a recording pulse generator that generates a recording pulse on the basis of a clock selected from the selector (Figure 1 element 18 and further in paragraph [0041]).

Iijima fails to teach a level shift stage that generates the plural fine clocks to be selected by the selector. AAPA, however, discloses the use of a level shift stage in the recording waveform generator (see Figure 13 element 22).

One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Iijima with AAPA because it would have been well known in the art at the time of the invention as shown in AAPA, to provide proper signal level for circuit operation. .

The combination of Iijima and AAPA discloses the claimed invention except for that the level shift stage is used after the selector. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the level shift stage prior to the selector, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Regarding claim 4, Iijima and AAPA teach a recording pulse generator as claimed in claim 1, wherein the selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks (see the discussion of the selector in Iijima paragraphs [0035]-[0039]). A selector is simply a switch that connects multiple lines to a single line and as such is equivalent to a multiplexer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made combine the teachings of Iijima and AAPA. One of ordinary skill in the art at the time the invention was made would have been motivated to incorporate the section taught by Iijima into the recording pulse generator of AAPA optimize the phase of the delay clock even when data is being recorded thus enabling the recording

waveform to be accurately generated even when the data is continuously recorded for a long time (see Iijima paragraph [0015]).

Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima (US PGPub 2002/0051415 A1) and AAPA as applied to claim 1 above, and further in view of Hayashi et al. (US Patent Number 6,493,305 B1).

Regarding claim 3, Iijima and AAPA fail to teach a recording pulse generator where the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed. Hayashi however, teaches a recording pulse generator wherein the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed (see Figures 1 and 3 and the teachings in column 5 lines 24-28 and column1 lines 40-42).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the use of the EFM clock input taught by Hayashi into the recording pulse generator of Iijima and AAPA because EFM reduces errors by minimizing the number of zero-to-one and one-to-zero transitions and small pits and lands are avoided. Disks can be played or written at different speeds; therefore the EFM data needs to be written to the disk at different speeds. As the speed increases, the period of the EFM signal decreases. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

Regarding claim 8, Iijima, AAPA, and Hayashi teach a recording pulse generator wherein the selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks (see the discussion of the selector in Iijima paragraphs [0035]-[0039]). A selector is simply a switch that connects multiple lines to a single line and as such is equivalent to a multiplexer.

Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima (US PGPub 2002/0051415 A1) and AAPA as applied to claim 1 above, and further in view of Kobayashi et al. (US Patent Number 5,818,805).

Regarding claims 5 and 12, Iijima and AAPA fail to teach a recording pulse generator provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer. Kobayashi, however, teaches a recording pulse generator wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer (see the recording signal generating apparatus which uses a T-type flip-flop triggered by the output of a data selector Figure 16 element 18 and column 12 lines 50 and 51; the data selector provides one of eight delayed clock outputs to the T-type flip-flop see Figure 16 element 10 and column 12 lines 28-36).

One of ordinary skill in the art, at the time the invention was made, would have been motivated to combine the teachings of Iijima and AAPA with Kobayashi and would have had a reasonable expectation in producing the claimed invention because Iijima, AAPA, and Kobayashi teach analogous art. Specifically, it would have been obvious to

one of ordinary skill in the art, at the time the invention was made, to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima. It would have been advantageous to use an integrated circuit, such as a flip-flop, versus combining AND and NAND gates to perform the desired function of the recording waveform generator. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima (US PGPub 2002/0051415 A1), AAPA, and Hayashi et al. (US Patent Number 6,493,305 B1) and further in view of Kobayashi et al. (US Patent Number 5,818,805).

Regarding claims 11 and 15, Iijima, AAPA, and Hayashi fail to teach a recording pulse generator provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer. Kobayashi, however, teaches a recording pulse generator wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer (see the recording signal generating apparatus which uses a T-type flip-flop triggered by the output of a data selector Figure 16 element 18 and column 12 lines 50 and 51; the data selector provides one of eight delayed clock outputs to the T-type flip-flop see Figure 16 element 10 and column 12 lines 28-36).

One of ordinary skill in the art, at the time the invention was made, would have been motivated to combine the teachings of Iijima, AAPA and Hayashi with Kobayashi and would have had a reasonable expectation in producing the claimed invention because Iijima, AAPA, Hayashi and Kobayashi teach analogous art. Specifically, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima. It would have been advantageous to use an integrated circuit, such as a flip-flop, versus combining AND and NAND gates to perform the desired function of the recording waveform generator. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

(10) Response to Argument

Appellant's arguments, beginning on page 8 of the Appeal Brief, filed October 29, 2007, have been fully considered but they are not persuasive.

Appellant argues the Examiner has erroneously characterized the background disclosure in the specification as Appellants' Admitted Prior Art. Appellant contends that there is no admission of "prior art," the case law is contrary to Examiner's position, and that there is no identified statutory support.

While Appellant argues that the "Description of Related Art" section does not qualify as statutory prior art because it is not labeled "Prior Art" and that the text refers to the structure as "conventional" and never uses the term "prior art," Examiner asserts

that labeling the text "Description of the Related Art" verses "Description of the Prior Art" is merely an exercise in form over substance. Since the relevant text repeatedly refers to the structure as "conventional," which is defined by Encarta dictionary as "using well established methods or styles," all text and figures refered to as conventional in the section labeled "Description of the Related Art" are considered prior art by the Examiner.

Further, Appellant argues that there is no identified statutory support and that the Examiner does not state under what statutory basis the Appellant's disclosure qualifies as prior art. However, as indicated in the MPEP, "admitted prior art can be relied upon for both anticipation and obviousness determinations, regardless of whether the admitted prior art would otherwise qualify as prior art under the statutory categories of 35 U.S.C. 102" (MPEP § 2141.01, section I, and MPEP § 2129. *Riverwood Int'l Corp. v. R.A. Jones & Co.*, 324 F.3d 1346, 1354, 66 USPQ2d 1331, 1337 (Fed. Cir. 2003)). While the Examiner is fully aware that where the inventor continues to improve upon his own work, the work of the same inventive entity may not be considered prior art against the claims, the Appellant has failed to provide appropriate evidence indicating that the admitted prior art is that of the same inventive entity.

Regarding claim 1, Appellant's arguments have been fully considered but they are not persuasive.

Initially, Appellant improperly characterizes Examiners rejection of claim 1 by indicating that Examiner relies on elements of Figure 3 of the Iijima reference. While

the Examiner does in fact make reference to Figure 1 of the Iijima reference, nowhere in the Final Office Action does the Examiner refer to Figure 3 of the Iijima reference.

Appellant further misrepresents the Examiner's rejection of claim 1 by assuming that "the Examiner considers the delay line to be element 11a and the selector to be element 12 in Fig. 13." The Examiner respectfully disagrees with Appellants assumption. In the rejection of claim 1, Examiner clearly indicates that the delay line and the selector are respectively represented by elements 11 and 12 of Figure 1. Further, the Iijima reference does not contain a drawing labeled Figure 13.

On page 12 of the Appeal Brief Appellant also notes that an embodiment of Figure 13 contains a phase adjustment section 40 receives a clock signal at a PLL circuit 41 and provides it to a shift register 42 and selector 43 prior to input delay line 11 and selector 12. Again, the Iijima reference does not contain a drawing labeled Figure 13 and while Figure 3 contains the noted elements, nowhere in the Final Office Action does the Examiner refer to Figure 3 of the Iijima reference.

Appellant argues that the Examiner points to the Iijima reference for teachings of a delay line generating plural fine clocks, however, Appellant again incorrectly refers to the Examiners rejection of claim 1 stating that the Examiner "points to the disclosure in paragraphs [0014] and [0033] as containing the pertinent teachings" and further misquotes the Examiner as pointing to the delay line as being equivalent to a structure that "generates plural fine clocks." However, the rejection of claim 1 cites paragraph [0041] of the Iijima reference and indicates that the first delay line "outputs plural output clocks" versus the "plural fine clocks" improperly quoted by Appellant.

Appellant then notes that claim 1 defines the delay line as producing output signals and the level shift stage as producing fine clocks and refers to the specification to illustrate the difference by citing "Although the conventional recording pulse generator implements the OR operation of the selected clock from the delay line 11 and the EFMDATA-1T to attain the recording pulse, the recording pulse generator of this embodiment delays the EFMCLK by the delay line 11, namely, generates a delayed signal (fine clock) of the EFMCLK by utilizing the ring oscillator VCO composed of the inverter 2b, as described above, and controls a recording pulse generator 25 by the signal (fine clock) to generate a recording pulse." In response to Appellant's argument that the references fail to show certain features of Appellant's invention, it is noted that the features upon which Appellant relies (i.e., the EFMCLK and "generating a delayed signal (fine clock) of the EFMCLK by utilizing the ring oscillator VCO composed of the inverter 2b) are not recited in rejected claim 1. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

With regard to Appellant's arguments beginning on page 13 of the Appeal Brief, Appellant argues that "there is no teaching that the clocks in the Iijima reference are having different phase differences with a clock inputted to the first phase of the delay line, according to the number of stages of the plural circuit elements thereof." Examiner respectfully disagrees. As noted in the rejection of claim 1, Figure 1 element 11 and the discussion regarding the delay line in paragraph [0033] of Iijima clearly disclose the claimed feature. Paragraph [0033] of Iijima states "a delay line 11 has a plurality of

delay elements 11a connected in series with each other. Each delay element 11a outputs an input signal with a prescribed delay time. The delay line 11 receives the first clock signal SCK1 and outputs the respective outputs of the delay elements 11a as a delay clock signal group SCK2. In other words, the delay clock signal group SCK2 is a set of signals each having a different phase difference from the first clock signal SCK1."

Appellant further argues that a level shift stage would not be an inherent feature of Iijima and in the absence of the level shift stage Iijima is clearly distinguishable from the claimed invention. In response to Appellant's arguments against the Iijima reference individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellant additionally argues that the level shift stage (Figure 13 element 22 of AAPA) does not teach or suggest that the level shift stage may be used to generate fine clocks to be selected by the selector and again argues that "the recording pulse generator of this embodiment delays the EFMCLK by the delay line 11, namely, generates a delayed signal (fine clock) of the EFMCLK by utilizing the ring oscillator VCO composed of the inverter 2b, and controls a recording pulse generator 25 by the signal (fine clock) to generate a recording pulse." Appellant's arguments are merely regarding the placement of the level shift stage. While Examiner admits the lack of the level shift stage in Iijima, both Iijima and AAPA teach recording waveform generators each of which utilizes a delay line having plural circuit elements selectors to generating

plural output clocks. As indicated in the Final Office Action, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Iijima with AAPA because it would have been well known in the art at the time of the invention as shown in AAPA (i.e. the use of level shifting in recording waveform generation would have been well known in the art at the time of the invention), to provide proper signal level for circuit operation.

As such, the combination of Iijima and AAPA disclose the claimed invention except for that the level shift stage is used after the selector. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the level shift stage prior to the selector, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

The claimed invention utilizes a delay line to generate plural output clocks, utilizes the level shift stage to generate plural fine clocks, selects a fine clock from the plural fine clocks and utilizes the selected fine clock to generate a recording pulse while AAPA discloses a delay line to generate plural output clocks, selecting a clock from the plural clocks, utilizing a level shift stage to generate a fine clock from the selected clock and generating a recording pulse from the fine clock. Whether the level shifting occurs before or after clock selection is inconsequential because ultimately, both the claimed invention and the combination of the prior art disclose generating a recording pulse from a fine clock which is derived from plural output clocks.

Regarding claim 4, Appellant's arguments have been fully considered but they are not persuasive.

Appellant improperly characterizes Examiners rejection of claim 4 by indicating that the Examiner relies on paragraph [0014] for the disclosure of a selector selecting one delay clock signal from the delay clock signal group and for teaching of the function that the selection signals are shifted in the same phase with the fine clocks. Appellant further argues that a multiplexer is expressly required and that while the Examiner states that the selector in Iijima is equivalent, there is no description by the Examiner of how there is equivalence to a multiplexer. However, as noted in the rejection of claim 4 in the Final Office Action, Examiner refers to paragraphs [0035]-[0039] for the pertinent teachings and not paragraph [0014] as Appellant improperly states. Further, contrary to Appellants assertion that no description of how the selector of Iijima equates to a multiplexer, the examiner cites the pertinent teachings of the selector whose selection is controlled based on a signal that is shifted in the same phase with the clocks in paragraphs [0035]-[0039]. In addition the Examiner does in fact state the definition of a selector which operates the same as the claimed multiplexer.

Regarding claims 2, 6, 7, and 9, Appellant's arguments, beginning on page 14 of the Appeal Brief, filed October 29, 2007, have been fully considered and are persuasive. The rejections of claims 2, 6, 7, 9, 10, 13, 14, and 16 have been withdrawn.

Regarding claims 5 and 12, Appellant's arguments have been fully considered but they are not persuasive.

Appellant argues that claims 5 and 12 are patentable for the reasons given for their parent claims. However, Examiner asserts that claims 5 and 12 are not patentable at least for the reasons indicated in the rejection of the parent claims and further because Kobayashi teaches a recording pulse generator wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer (see the recording signal generating apparatus which uses a T-type flip-flop triggered by the output of a data selector Figure 16 element 18 and column 12 lines 50 and 51; the data selector provides one of eight delayed clock outputs to the T-type flip-flop see Figure 16 element 10 and column 12 lines 28-36).

One of ordinary skill in the art, at the time the invention was made, would have been motivated to combine the teachings of Iijima and AAPA with Kobayashi and would have had a reasonable expectation in producing the claimed invention because Iijima, AAPA, and Kobayashi teach analogous art. Specifically, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima. It would have been advantageous to use an integrated circuit, such as a flip-flop, versus combining AND and NAND gates to perform the desired function of the recording waveform generator. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

Regarding claims 3 and 8, Appellant's arguments have been fully considered but they are not persuasive.

Appellant argues that claims 3 and 8 are patentable for the reasons given for their parent claims. However, Examiner asserts that claims 3 and 8 are not patentable for the reasons indicated above.

Regarding claims 11 and 15, Appellant's arguments have been fully considered but they are not persuasive.

Appellant argues that Kobayashi does not teach how and why a combination of the distinct structures of Hayashi should be inserted into the structure of Iijima and that it is the combination of components in the claims is not taught or suggested in the prior art, other than to the Examiner's use of hindsight.

As indicated in the rejections of claims 11 and 15 while the combination of Iijima, AAPA, and Hayashi fail to teach a recording pulse generator provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer. Kobayashi, however, teaches a recording pulse generator wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer (see the recording signal generating apparatus which uses a T-type flip-flop triggered by the output of a data selector Figure 16 element 18 and column 12 lines 50 and 51; the data selector provides one of eight delayed clock outputs to the T-type flip-flop see Figure 16 element 10 and column 12 lines 28-36).

One of ordinary skill in the art, at the time the invention was made, would have been motivated to combine the teachings of Iijima, AAPA and Hayashi with Kobayashi and would have had a reasonable expectation in producing the claimed invention because Iijima, AAPA, Hayashi and Kobayashi teach analogous art. Specifically, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima. It would have been advantageous to use an integrated circuit, such as a flip-flop, versus combining AND and NAND gates to perform the desired function of the recording waveform generator. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

In response to Appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the Appellant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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